STUDY AND ANALYSIS OF LOW POWER TRANSISTOR LEVEL 1-BIT FULL ADDER CELLS AND COMPATISON OF THEIR POWER EFFICIENCIES

Bhaskar Sarkar[1], Dhrubajyoti Adak[2], Prof.Rajib Pal[3], Prof.Uttam Kumar Dey[4]
bhaskarsarkar222@gmail.com[1], adakdhrubajyoti@gmail.com[2],rajib.pal123@gmail.com[3], ukd2006@rediffmail.com[4]
Electronics and Communication Engineering,
Camellia Institute of Technology, Madhyamgram, Kolkata – 700129.

Abstract -In this paper, different designed adders are studied and analysed. Analysis is based on some simulation parameters like power, delay and power-delay-product (PDP), different technologies, number of transistor. Simulation is done by HSPICE in 0.18µm CMOS Technology at 1.8 V supply voltage. The different circuit designs are studied and evaluated extensively. Simulations of several designs give new information which are applicable for different requirements. Each of these circuits cell exhibits different power consumption, delay and power-delay- product in different VLSI technology. This paper can be said as a library of different full adder circuits that will be beneficial for the circuit designers to pick the full adder cell that satisfied their specific application.

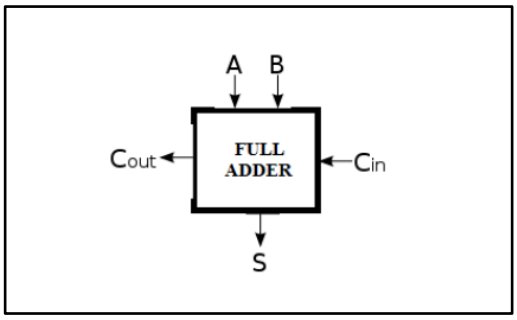
Keywords - CCMOS, 14T Adder, SERF, GDI, PDP, PTL.

1 Introduction

The extensive development in the field of portable systems and cellular networks has intensified the research efforts in low-power microelectronics. The low-power design has become a major design consideration. Designing low-power VLSI system is significant because of the fast growing technology in mobile computation and communication. Today, we find the number of portable applications requiring low power and high throughput circuits. The design criterion of a full adder cell is usually multi-fold. Full adders are fundamental cell in various circuits which is used for performing arithmetic operations such as addition, subtraction, multiplication, address calculation and MAC unit etc. Addition is one of the fundamental arithmetic operations. It is used extensively in many VLSI systems such as application specific DSP architectures and microprocessors. Transistor count is, of course, a primary concern which largely affects the design complexity of many function units such as multiplier and algorithmic logic unit.

There is no ideal full adder that can be used in all types of applications [1]. In this paper, we have given a brief description of evolution of full adder circuits in terms of lesser power consumption, higher speed, lesser chip size and higher efficiency. Hence, novel architectures such as CMOS Transmission Gate (TG), Pass-Transistor Logic (PTL), Complimentary Pass-Transistor Logic (CPL) [2] and Gate Diffusion Input (GDI) [3] are proposed to meet the requirements. Each design style has its own share of advantages and disadvantages. We have started with the most conventional 28 transistor full adder and then gradually studied full adders consisting of as less as 14 transistors (14T), 16 transistors (16T), CMOS Transmission Gate (TG), Complimentary Pass-Transistor Logic (CPL) [2], Gate Diffusion Input [4] and Static Energy Recovery Full Adder (SERF) are proposed to meet the requirements.

2 Architecture of Adder



The logic for the Complimentary MOS Logic was realized using the below equations:

$C_{out} = AB + BC_{in} + AC_{in}$

$Sum = ABC_{in} + (A+B+C_{in})C'_{out}$

3 Overview of Power Dissipation

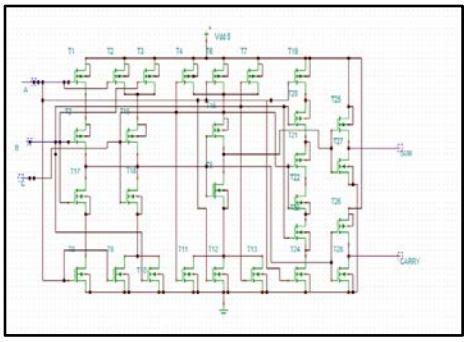
Power dissipation in CMOS digital circuits is categorized in two types: peak power and time-averaged power consumption. Peak power is a reliability issue that determines both the chip lifetime and performance. The

voltage drop effects caused by the excessive instantaneous current flowing through the resistive power network affects the performance of a design due to the increased gate and interconnect delay. This large power consumption causes the device to overheat which reduces the reliability and lifetime of the circuit. Also noise margins are reduced, increasing the chance of chip failure due to cross-talk. The time-averaged power consumption in conventional CMOS digital circuits occur in two forms: dynamic and static. Dynamic power dissipation occurs in the logic gates that are in the process of switching from one state to another. During this process, any internal and external capacitance with the gate's transistor has to be charged, thereby consuming power.

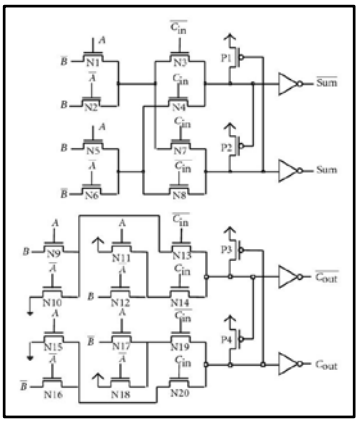
Static power dissipation is associated with inactive logic gates (i.e., not currently switching from one state to another). Dynamic power is important during normal operation, especially at high operating frequencies, whereas static power is more important during standby, especially for battery-powered devices. Dynamic dissipation has historically been far greater than static power when the system are active, and hence static power is often ignored, although this will change as great and sub-threshold leakage increases.

4 Comparison of different Full Adders

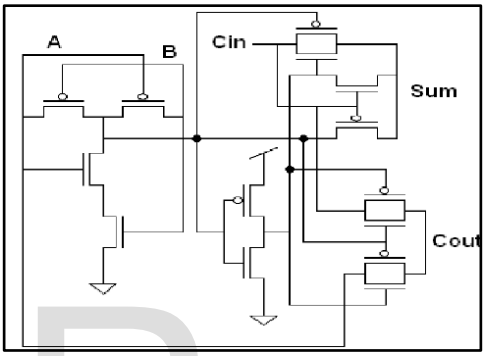
4.1 Conventional 28T Full Adder: This adder was based on regular CMOS structure (pull-up and pull-down network).



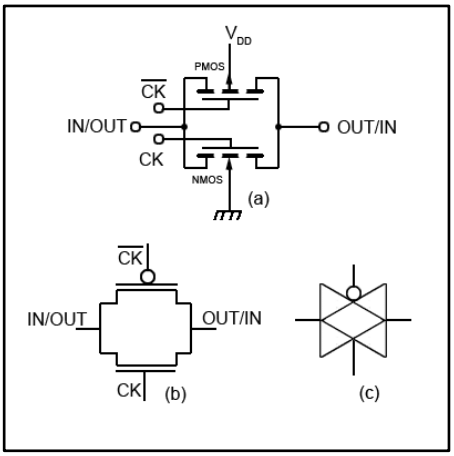
4.2 Complimentary Pass-Transistor Logic (CPL): The Complimentary Pass-Transistor Logic (CPL) Full Adder is shown below. This contains 18 transistors that based on NMOS pass-transistor network. CPL adder provides low input capacitance and less output voltage swing that is the result of one threshold voltage, V_t loss in the output.



4.314T Full Adder: The 14T full adder contains a 4T PTL XOR gate, an inverter and two transmission gates based multiplexer designs for sum and C_{out} signals [5].

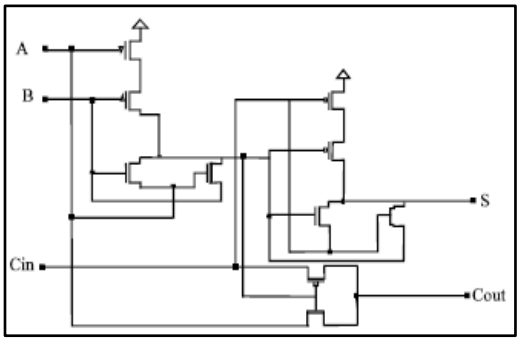


4.4CMOS Transmission Gate (TG): Transmission gate logic circuit is a special kind of pass-transistor logic circuit. It is built by connecting a PMOS transistor and a NMOS transistor in parallel, which are controlled by complimentary control signals.

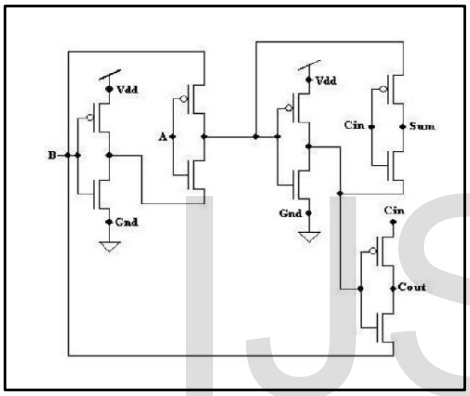


4.5 Static Energy Recovery Full Adder (SERF):In this type of adder, the energy recovering logic reuses charge and therefore consumes less power than non-energy recovering logic. The circuit consists of two XNORs realized by 4 transistors. Sum is generated from the output of the second stage XNOR circuit. The C_{out} can be

calculated by multiplexing A and C_{in}controlled by (AXOR B).



4.6 Gate Diffusion Input: The circuit operation of GDI based full adders, is exactly the same as that of previous SERF module. Sum bit is obtained from the output of the second stage of XOR circuit while carry bit (C_{out}) is calculated by B and C_{in} controlled by (A XNOR B).



5 Comparison of PDP of different Adders

Parameters	CCMOS Adder	CPL Adder	14T Adder	CMOS TG Adder	SERF Adder	GDI Adder
Number of Transistors	28	18	14	20	10	10
Average Power (W)	3.81*E-07	4.57*E-07	2.93*E-02	3.59*E-07	1.50*E-10	1.01*E-06
Delay (s)	1.88*E-10	1.72*E-10	7.47*E-10	7.81*E-11	8.73*E-09	9.71*E-11
PDP (J)	7.16*E-17	7.86*E-17	2.18*E-11	2.80*E-17	1.31*E-18	9.81*E-17

6 Conclusion

From the above data collected by comparing the Power Delay Product of different adders, we can see that the lowest or the least PDP is of the Static Energy Recovery Full Adder (SERF), which has PDP of 1.31*E-18. So, from this we can conclude that the efficiency of the SERF adder is highest compared to the other different adders.

7 References

[1] A. A. Khatibzadeh and K. Raahemifar, "A Study and Comparison of Full Adder Cells based on the Standard Static CMOS Logic.", IEEE CCECE 2004 - CCGEI 2004, Niagara Falls, May 2004.

[2] S. M. Kang and Y. Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", Third Edition, Tata McGraw-Hill Edition 2003, pp 307-316.

[3] J. H. Kang and J. B. Kim, "Design of a Low Power CVSL Full Adder Using Low-Swing Technique", ICSE2004 Proc. 2004, Kuala Lumpur, Malaysia.

[4] A. Morgenshtein, A. Fish and A. Wagner, —Gate-Diffusion Input(GDI): A Power-Efficient Method for Digital Combinational Circuits‖, IEEE Trans.VLSI Syst., pp. 566-581, Oct. 2002.

[5] J. Wang, S. Fang, and W. Feng, "New efficient designs for XOR and XNOR functions on the transistor level", IEEE J. Solid-State Circuits, vol. 29, no. 7, Jul. 1994, pp. 780–786.